What is claimed is:

1. A device comprising:

a plurality of data lines for transferring both data and auxiliary information;

a memory array for storing the data;

an auxiliary circuit having auxiliary lines for carrying auxiliary information; and

a transceiver circuit connected to the memory array and the data lines for transferring the data between the memory array and the data lines, the transceiver circuit also connects to the auxiliary circuit for transferring the auxiliary information between the auxiliary lines and the data lines.

2. The device of claim 1, wherein the auxiliary circuit includes an inversion controller connected to the transceiver circuit and the memory array for conditionally inverting the data.

3. The device of claim 2, wherein the auxiliary circuit further includes a parity controller connected to the transceiver circuit and the memory array for generating a number of parity codes for the data.

4. The device of claim 3, wherein the auxiliary circuit further includes a temperature reporting circuit connected to the transceiver circuit for generating temperature information of the device.

5. The device of claim 4, wherein the auxiliary circuit further includes a calibrating circuit connected to the transceiver circuit for providing a time delay based on the auxiliary information.

6. A device comprising:

a plurality of data lines;

a memory array for storing data;

an auxiliary circuit including a parity controller connected to the memory array for generating a plurality of parity codes for the data; and

a transceiver circuit connected to the memory array and the data lines for transferring the data between the memory array and the data lines, the transceiver circuit also connects to the parity controller for transferring the parity codes between the parity controller and the data lines.

7. The device of claim 6, wherein the parity controller includes a number of comparators for comparing bits of the data.

8. The device of claim 7, wherein the parity controller includes a storage unit for storing the parity codes.

9. The device of claim 6, wherein the auxiliary circuit further includes an inversion controller connected to the transceiver circuit and the memory array for conditionally inverting the data transferred between the transceiver circuit and the memory array.

10. The device of claim 9, wherein the inversion controller includes a storage unit for storing inverting codes of the data, and wherein the transceiver circuit connects to the storage unit for transferring the inverting codes between the inverting parity controller and the data lines.

11. A device comprising:

a plurality of data lines;

a memory array for storing input data and output data;

an input auxiliary circuit configured for receiving input auxiliary information of the input data and configured for performing a function on the input data;

an output auxiliary circuit configured for generating output auxiliary information of the output data and configured for performing a function on the output data; and

a transceiver circuit connected to the memory array and the data lines for transferring the input and output data between the memory array and the data lines, the transceiver circuit also connects to the input and output auxiliary circuits for transferring the input and output auxiliary information between the input and output auxiliary circuits and the data lines.

12. The device of claim 11, wherein the output auxiliary circuit includes an output inverting circuit for conditionally inverting the output data based on the output auxiliary information.

13. The device of claim 12, wherein the output auxiliary circuit further includes an output parity generator for generating a number of parity codes for the output data.

14. The device of claim 13, wherein the output auxiliary circuit further includes a temperature reporting circuit for generating temperature information of the device.

15. The device of claim 14, wherein the input auxiliary circuit includes an input inverting circuit for conditionally inverting the input data based on the input auxiliary information.

16. The device of claim 15, wherein the input auxiliary circuit further includes an input parity generator for generating a number of parity codes for the input data.

17. The device of claim 16, wherein the input auxiliary circuit further includes a calibrating circuit for providing a time delay based on the input auxiliary information.

18. A system comprising:

a controller; and

a memory device connected to the controller, one of the controller and the memory device including:

a plurality of external terminals;

a memory array for storing data;

an auxiliary circuit having auxiliary lines for carrying auxiliary information; and

a transceiver circuit connected to the memory array and the external terminals for transferring the data between the memory array and the external terminals, the transceiver circuit also connects to the auxiliary circuit for transferring the auxiliary information between the auxiliary lines and the external terminals.

19. The system of claim 18, wherein the auxiliary circuit includes an inversion controller connected to the transceiver circuit and the memory array for conditionally inverting the data.

20. The system of claim 19, wherein the auxiliary circuit further includes a parity controller connected to the transceiver circuit and the memory array for generating a number of parity codes for the data.

21. The system of claim 20, wherein the auxiliary circuit further includes a temperature reporting circuit connected to the transceiver circuit for generating temperature information of one of the controller and the memory device including.

22. The system of claim 21, wherein the auxiliary circuit further includes a calibrating circuit connected to the transceiver circuit for providing a time delay based on the auxiliary information.

23. A method comprising:

transferring a number of groups of data bits on a plurality of data lines, the data bits having a first type of data;

transferring a plurality of auxiliary bits on the data lines, the auxiliary bits having a second type of data;

performing a first function on bits of each of the groups of data bits; and

performing a second function on the auxiliary bits.

24. The method of claim 23, wherein the auxiliary bits represent a plurality of inverting codes for the groups of data bits.

25. The method of claim 23, wherein the auxiliary bits represent a plurality of parity codes the groups of data bits.

26. The method of claim 23, wherein the auxiliary bits represent a temperature information.

27. The method of claim 23, wherein the auxiliary bits represent time delay information.

28. The method of claim 23, wherein the first function is conditionally inverting bits of the groups of data bits.

29. The method of claim 23, wherein the first function is comparing bits within each of the groups of data bits.

30. The method of claim 23, wherein the second function is decoding the auxiliary bits to generate a temperature information.

31. The method of claim 23, wherein the second function is decoding the auxiliary bits to generate a time delay information.

32. The method of claim 23, wherein transferring the groups of data bits occurs before transferring the auxiliary bits.

33. The method of claim 23, wherein the number of groups of data bits is a multiple of two.

34. A method comprising:

transferring a number of groups of data bits between a memory array and a plurality of data lines;

transferring a number of groups of auxiliary bits on the data lines, wherein at least one of the groups of auxiliary bits represents auxiliary information of the groups of data bits;

performing a first function on bits of each of the groups of data bits; and

performing a second function on bits of each of the groups of auxiliary bits.

35. The method of claim 34, wherein each bit of a first group of auxiliary bits represents an inverting code for one of the groups of data bits.

36. The method of claim 35, wherein each bit of a second group of auxiliary bits represents a parity code for one of the groups of data bits.

37. The method of claim 36, wherein a combination of bits of a third group of auxiliary bits represents a temperature information.

38. The method of claim 37, wherein a combination of bits of a fourth group of auxiliary bits represents a time delay information.

39. The method of claim 34, wherein performing the first function includes conditionally inverting the bits of each of the groups of data bits.

40. The method of claim 39, wherein performing the first function includes comparing bits of each of the groups to generate a parity code for each of the groups of data bits.

41. The method of claim 40, wherein performing the second function includes decoding a combination of a first group of auxiliary bits to generate a temperature information.

42. The method of claim 41, wherein performing the second function includes decoding a combination of bits of a second group of auxiliary bits to adjust a propagation delay of data transferred on the plurality of data lines.

43. The method of claim 34, wherein at least one of the groups of auxiliary bits is transferred before the transferring of the number of groups of data bits.

44. A method comprising:

transferring a number of groups of data bits on a portion of a plurality of external terminals connected between a memory device and a controller;

transferring at least one group of auxiliary bits on the same portion of the plurality of external terminals; and

performing at least one function on bits of the groups of data bits.

45. The method of claim 44 further comprising:

transferring a second group of auxiliary bits; and

decoding the second group of auxiliary bits to obtain a temperature information.

46. The method of claim 44 further comprising:

transferring a second group of auxiliary bits; and

decoding the second group of auxiliary bits to obtain a time delay information.

47. The method of claim 44, wherein transferring the groups of data bits occurs before transferring all of the auxiliary bits.

48. A method comprising:

transferring a number of groups of data bits on a portion of a plurality of external terminals connected between a memory device and a controller;

transferring a plurality of inverting codes for the groups of data bits on the same portion of the plurality of external terminals; and

conditionally inverting bits of the groups of data bits.

49. The method of claim 48, wherein transferring the groups of data bits occurs before transferring the inverting codes.

50. A method comprising:

transferring a number of groups of data bits on a portion of a plurality of external terminals connected between a memory device and a controller;

transferring a plurality of parity codes for the groups of data bits on the same portion of the plurality of external terminals; and

comparing bits of the groups of data bits.

51. The method of claim 50, wherein transferring the groups of data bits occurs before transferring the parity codes.

52. A method comprising:

transferring a number of groups of data bits on a portion of a plurality of external terminals connected between a memory device and a controller;

transferring a plurality of temperature codes on the same portion of the plurality of external terminals; and

decoding the temperature codes to obtain a temperature information.

53. The method of claim 52, wherein transferring the groups of data bits occurs before transferring the temperature codes.

54. A method comprising:

transferring a number of groups of data bits on a portion of a plurality of external terminals connected between a memory device and a controller;

transferring a plurality of timing calibrating codes on the same portion of the plurality of external terminals; and

decoding the timing calibrating codes to obtain a time delay information.

55. The method of claim 54, wherein transferring the groups of data bits occurs before transferring the timing calibrating codes.